UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/629,966	07/31/2000	Moshe Gefen	246/68	4504

7590 11/12/2003

Dr. Mark Friedman Ltd
C/O BILL POLKINGHORN - DISCOVER DISPATCH
9003 FLORIN WAY
UPPER MARLBORO, MD 20772

EXAMINER	
ANDERSON, MATTHEW D	
ART UNIT	**PAPER NUMBER**
2186	4

DATE MAILED: 11/12/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/629,966	GEFEN ET AL.	
	Examiner	Art Unit	
	Matthew D. Anderson	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 July 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 July 2000* is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15)☒ Notice of References Cited (PTO-892)
16)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17)☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
18)☐ Interview Summary (PTO-413) Paper No(s). _____ .
19)☐ Notice of Informal Patent Application (PTO-152)
20)☐ Other: .

DETAILED ACTION

Drawings

1. The drawings are objected to because Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the external logic circuit of claims 7 and 9 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

3. A proposed drawing correction or corrected drawings are required in reply to this Office Action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

4. Claim14 is objected to because of the following informalities: the parentheses in "(automatically)" in line 7 should be deleted or the word deleted entirely . Appropriate correction is required.

5. Claim14 is objected to because of the following informalities: line 3 reads "..with *the a* non-volatile memory chip." The word "a" should be deleted. Appropriate correction is required.

6. Claim 15 is objected to because of the following informalities: claim 15 is listed as dependent upon claim 15. For examination purposes, claim 15 is treated as dependent upon claim 14. Appropriate correction is required.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 6-13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

9. Claims 6-7 recite the limitation "the memory chip." There is insufficient antecedent basis for this limitation in the claim.

10. Claims 8-9 recite the limitation "said logic circuits." There is insufficient antecedent basis for this limitation in the claim as plural logic circuits have not been previously claimed.

11. Claims 10 and 12-13 recite the limitation "said memory chip." There is insufficient antecedent basis for this limitation in the claim.

12. Claim 11 recites the limitation "the OS/application/file management software." There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

13. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

14. Claims 1-4 and 6-16 are rejected under 35 U.S.C. 102(e) as being anticipated by See *et al.* (US Patent # 6,189,070).

15. With respect to claims 1-3 and 13-14, See *et al.* disclose:

a CPU/Bus/Controller for controlling a non-volatile memory device, as shown by item 140 of figure 7;

a flash array for holding code and data, as disclosed in the abstract and column 1, lines 37-39;

non-volatile circuitry for controlling content and activity of the non-volatile array, as shown by the erase, program, and read circuitry (items 190, 194, and 196 of figure 7);

logic circuit hardware for enabling automatic suspending and/or automatic resuming of operations, as shown by the suspend circuitry (item 192 and 195 of figure 7).

16. With respect to claim 4, See *et al.* disclose the logic circuit enabling code execution and data storage/processing facilities within a single chip device with a single silicon die, as disclosed in the abstract and figure 5.

17. With respect to claims 6 and 8, See *et al.* disclose the logic circuit being embedded into a memory chip, as shown in figure 5.

18. With respect to claims 7 and 9, See *et al.* disclose logic circuit outside the memory chip, as shown by the processor (100) being external to the flash device (104) in figure 1.

19. With respect to claims 10 and 13, See *et al.* disclose the logic circuit monitoring the status of the current operations in the memory chip, as shown by the read status circuitry (item 198 in figure 7).

20. With respect to claims 11 and 15, See *et al.* disclose the logic circuit marking the current status of chip operation to make it readable, as shown by the read status circuitry (item 198 in figure 7).

21. With respect to claim 12, See *et al.* disclose the controller causing the memory chip to suspend and/or resume operations by signaling to the memory chip to delay read operation, by teaching in column 3, lines 15-25, enabling and disabling interrupts to allow read and non-read operations.

22. With respect to claims 13-14, See *et al.* additionally disclose signaling the CPU/bus if the chip is available for code execution, monitoring CPU/bus activity, and commanding the chip to suspend and/or resume chip operations, by teaching in column 3, lines 15-25, enabling and disabling interrupts to allow read and non-read operations, and a check for occurrences of interrupts.

23. With respect to claim 14, See *et al.* additionally disclose sensing read requests while the chip is in program/erase mode/operation, automatic entering of program and/or erase operations into suspend mode, signaling to the CPU/bus to wait before executing further read/fetch commands, turning off the signal to allow the CPU/bus to continue with read/fetch commands, and entering of the chip into resume operation to continue program/erase operation, as shown in figure 4A-4B.

24. With respect to claim 16, See *et al.* disclose suspend/resume logic circuitry for enabling hardware initiated suspending/resuming of data processing operations, as shown by the suspend circuitry (item 192 and 195 in figure 7).

Claim Rejections - 35 USC § 103

25. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

26. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over See *et al.* and Keeley *et al.* (US Patent # 4,491,790).

27. See *et al.* teach all other limitations of the parent claim, but fail to specifically disclose code execution and data storage/processing within a bank of single memory chips with single silicon dies. Keeley *et al.* teach in column 12, lines 5-8, of an EEPROM array with two banks which is used in a system which can suspend or resume processor operations.

28. It would have been obvious to one of ordinary skill in the art, having the teachings of See *et al.* and Keeley *et al.* before him at the time the invention was made, to modify the EPROM array in the system which can suspend or resume processor operations taught by See *et al.*, to be a banked EEPROM array, as with the system which can suspend or resume processor operations taught by Keeley *et al.*, to allow parallel access to the banks of the memory device, as taught by Keeley *et al.*.

Conclusion

29. The prior art made of record on form PTO-892 and not relied upon is considered pertinent to applicant's disclosure. Applicant is required under 37 C.F.R. § 1.111(c) to consider

these references fully when responding to this action. The documents cited therein teach similar non-volatile memory devices.

30. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew D. Anderson whose telephone number is (703) 306-5931.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim, can be reached on (703) 305-3821. The fax phone number for this Group is (703) 305-9731.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Matthew D. Anderson
November 3, 2003